REMARKS

Claims 1-39 are pending in this application.

Claims 4-23 have been previously withdrawn due to a restriction requirement.

Claims 1 and 24 have been rejected.

Claims 2, 3, and 25-32 have been objected to.

Claims 33-39 have been allowed.

Claims 1-39 remain pending in this application.

Reconsideration and full allowance of Claims 1-39 are respectfully requested.

I. ALLOWABLE SUBJECT MATTER

The Applicants thank the Examiner for the indication that Claims 2, 3, and 25-32 would be allowable if rewritten in independent form to incorporate the elements of their respective base claims and any intervening claims. Because the Applicants believe that the remaining claims in this application are allowable, the Applicants have not rewritten Claims 2, 3, and 25-32 in independent form at this time. The Applicants also thank the Examiner for the indication that Claims 33-39 have been allowed. Claims 33-39 have not been amended and therefore remain in condition for allowance.

II. REJECTION UNDER 35 U.S.C. § 102

Claim 1 and Claim 24 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,701,714 to A. Agoston (hereafter "*Agoston*"). The Applicants respectfully traverse these rejections.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Examiner stated that "Figure 1 of Agoston reference shows a phase shifter circuit comprising an input for receiving an input signal (input signal at node 12) having a specified oscillation frequency, an output delivering an output signal (14) having said specified oscillation frequency and having a variable phase shift with respect to said input signal, at least one control input receiving a control signal (20) which controls the phase shift of said output signal with respect to said input signal, and a synchronized oscillator (each S1 to Sn has oscillation frequency base on the valued of LCR and having output frequency similar to input frequency, thus anticipating the synchronized oscillator limitation) having at least a synchronization input coupled said input of said variable phase shifting circuit, at least one output coupled to said output of said output of the variable phase shifting circuit, said synchronized oscillator having a variable free running

oscillation frequency controlled by said control signal (the oscillation frequency of the ring oscillator is being controlled by the control signal) as called for in claims 1 and 24." (July 5, 2007 Office Action, Page 2, Lines 11-22).

The Applicants respectfully traverse these assertions for the reasons set forth below.

The *Agoston* reference discloses an electrically tunable delay line 10 that comprises an input terminal 12, an output terminal 14 and a control terminal 20. The input terminal receives a signal to be delayed. The control terminal 20 receives a control or tuning voltage Vt. The delay line 10 comprises a plurality of "n" delay line sections (S_1, S_2, S_3, ... S_{n-1}, S_n). Each delay line section comprises an inductor (L) and a capacitor (C) and a resistor (R) and a variable capacitance diode (D). For example, delay line section S1 comprises inductor L_1, capacitor C_1, resistor R_1 and variable capacitor diode D1 connected together as shown in Figure 1 of the *Agoston* reference. Each of the "n" delay line sections (S_1, S_2, S_3, ... S_{n-1}, S_n) introduces a delay in the transmission of the signal that is input at the input terminal 12. The delayed signal is output at the output terminal 14.

Neither the delay line 10 that is shown in Figure 1 nor the delay line 30 that is shown in Figure 3 of the *Agoston* reference comprises an oscillator. None of the individual delay line sections of delay line 10 (i.e., S_1, S_2, S_3, ... S_{n-1}, S_n) comprises an oscillator. None of the individual delay line sections of delay line 30 (i.e., S_1', S_2', S_3', ... S_{n-1}', S_n') comprises an oscillator.

An oscillator may comprise a delay line. However, a delay line does not necessarily comprise an oscillator. Each of the individual delay line sections (S) described in the *Agoston* reference differs from an oscillator. A resistor-inductor-capacitor (RLC) circuit does not

necessarily form an oscillator. In order for an RLC circuit to oscillate, the RLC circuit must be provided a periodic excitation signal that has a frequency that is close to the resonance frequency of the RLC circuit. The individual delay line sections (S) of the delay line 10 that are described in the *Agoston* reference are not used as oscillators at all. In addition, the individual delay line sections (S') of the delay line 30 that are described in the *Agoston* reference are also not used as oscillators at all.

In addition, the control signal at terminal 20 of the delay line 10 does not control the phase-shift of the output signal of the delay line 10 with respect to the input signal. The control signal at terminal 50 of the delay line 30 does not control the phase-shift of the output signal of the delay line 30 with respect to the input signal. The control signal at terminal 20 (and the control signal at terminal 50) is applied to the variable capacitance diodes in order to vary the delay of the input signal that is traversing the delay line. (*Agoston*, Claim 2).

For these reasons, the delay line 10 (and the delay line 30) of the *Agoston* reference does not anticipate the Applicants' invention as claimed in Claims 1 and 24. Accordingly, the Applicants respectfully request withdrawal of the §102 rejections and full allowance of Claim 1 and Claim 24.

III. CONCLUSION

For the foregoing reasons, the Applicants respectfully request full allowance of all pending claims and that this application be passed to issuance.

The Applicants' attorney has made the amendments and arguments set forth above in order to place this application in condition for allowance. In the alternative, the Applicants' attorney has made the amendments and arguments to properly frame the issues for appeal. The Applicants make no admission concerning any now moot rejection or objection, and affirmatively denies any position, statement or averment of the Examiner that was not specifically addressed herein.

SUMMARY

The Applicants respectfully assert that all pending claims in this application are in condition for allowance and respectfully request that this application be passed to issue.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@munckbutrus.com.*

The Commissioner is hereby authorized to charge any necessary fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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